UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,594	07/16/2003	Tomohiko Otose	8070-1001	7456

466 7590 06/21/2005

YOUNG & THOMPSON
745 SOUTH 23RD STREET
2ND FLOOR
ARLINGTON, VA 22202

EXAMINER	
NGUYEN, VIET Q	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 06/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,594	OTOSE, TOMOHIKO	
	Examiner	Art Unit	
	Viet Q. Nguyen	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Election filed on 3/29/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29 and 57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *5,8,11,17,20 and 23* is/are allowed.

6)☒ Claim(s) *1-4,6,7,9,10,12-16 and 57* is/are rejected.

7)☒ Claim(s) *18,19,21,22 and 24-29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims **1-29 and 57** are present for examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims **1-4, 6-7, 9-10, 12-13, 15-16, and 57** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Feldman et al (6,582,980).**

Regarding both claims **1 & 4**, Feldman et al (see Fig. 3) clearly shows a semiconductor device formed on a common substrate (12, see col. 4) which includes the following claimed elements: a memory unit (frame buffer 40) having plurality of addresses for temporarily storing a data signal (or image signal) to be displayed, a functional element (or image display panel 11), a data signal providing unit (see input interface 44) for providing said data signal (from external input data) into said memory unit (buffer 40) through the use of a digital image processing circuit (42), and a driving unit (display driver 30) for generating a control signal (16) for controlling such functional element (or image display device 11) based on the data signal read out from said temporary memory unit (buffer 40, 43) and providing said control signals 916) to said functional element

(image display 11). It is noted that the so-called "control circuit (46)" appeared in Fig. 3 also act equivalently as the claimed "data-update control unit" for successively providing the same image data (or signal) from the memory buffer (40) onto the display driver (30) and finally onto the display device (11) as well. In regard to the claimed limitation of "***identical data signal over a plurality of times from an identical address in said memory***", it is noted that Feldman reference does not clearly stated so. However, it is the examiner's position that Feldman did suggest that a same, still image data can be displayed onto the image display by the "refresh" operation over plurality of times, and that such still, same image data is obviously considered by one skilled in this art as an "identical image/data" fetched from a same/ identical addressed location from a memory as well. The reason is because this reference (see col. 10, lines 16-20) specifically imply that "***for still image, the digital image data passes through the digital image processing circuit (42) only once, no matter how many times the same digital image data is used to refresh the image display (11). The display refreshes use digital image data read from the frame buffer (40)***". Thus, it would be further obvious from this statement that such same or identical image, if any, should be stored in the memory buffer (40) at one same location or identical address, and it is used over a plurality of times for the display refresh operation as also well-known by every artisan in this art.

Regarding claims **2 & 3**, Feldman et al (see col. 12, lines 4-20) discusses the function of the data update-control circuit (46) in order to control the overall operation of the whole circuitry within the display module (10). It also stated ***"... the control circuit 46 allows the display module (10) to refresh the image display (11) without any intervention from circuitry external to the display module".*** Therefore, any external data signal from the outside of memory buffer unit (40) is obviously suspended from supply operation as well, thus also it would obviously keep the same/identical image data from being updated during the refresh operation as claimed.

Regarding claims **6-7, 9-10**, it would be obvious from Fig. 3 that said driving unit (30), said memory unit (40), said functional element (display 11), and also said data update control unit (46) are all located in one single substrate device or so-called "combined unit" as well.

Regarding claims **12 & 13**, Fig. 3 shows the "imputer interface (44) and processing circuit (42)" as claimed "first signal transferring unit" for transferring data signal from external host devices/sensors (see also Figs. 9-11) into the memory unit (40), and the "control circuit 946) as claimed "second signal transferring unit" for transferring said data signal from memory unit to the driver (30).

Regarding claims **15 & 16**, Figs. 9-11 all show the uses of associated circuitry (i.e., amplifier, mod/demod, and pulse shaping, etc.) for transforming and/or converting the amplitude of input signals into said input interface and also into the memory unit at desired amplitude.

Regarding claim **57**, as pointed out above, Feldman et al obviously suggest a 'refresh" operation in which a same, identical image data fetched from a same, identical addressed location is also "temporarily stored" in the memory unit (buffer) and "being used successively" over times as claimed.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims **12-14, 24-26** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 12-14, it is unclear what is meant by "said second signal transferring unit ***is shorter than*** said first unit"? Does it imply that the "output signals" generated from these nits being compared with each other, or does it imply that the "physical dimensions" of each unit as being compared to each other? Clarifications and/or claim revision is requested.

In claims **24-26**, said "first and second transferring units" lack proper antecedent basis from their parent claims, which certainly make these claims more confusing. Clarification and/or revision is requested.

5. Claims **5, 11, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27-29** contain allowable subject over prior arts of record with regard to at least one or more of the following claimed features of, e.g., "first driving unit for external control signal from outside", second driving unit", "serial/parallel converter unit for input operation", and "thin film transistor constituted of poly material", etc.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Viet Q. Nguyen whose telephone number is (571) 272-1788. The examiner can normally be reached on 7am-6pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

V. Nguyen
6/12/2005

Viet Q Nguyen
Primary Examiner
Art Unit 2827